CLEAN COPY OF ALL PENDING CLAIMS

1. A method of fabricating a semiconductor device comprising:

(a) providing a semiconductor heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer on said strained channel layer;

A1 (b) chemically reacting at least a portion of said $Si_{1-y}Ge_y$ layer to form a chemically modified $Si_{1-y}Ge_y$ layer on said strained channel layer;

(c) removing said chemically modified $Si_{1-y}Ge_y$ layer to expose said strained channel layer; and

(d) providing a dielectric layer on said exposed strained channel layer.

A2 2. ~~3.~~ The method of claim 1 wherein step (b) comprises oxidizing said at least a portion of said $Si_{1-y}Ge_y$ layer.

A3 3. ~~5.~~ The method of claim 1 wherein said dielectric layer comprises a gate dielectric of a MISFET.

4. ~~10.~~ The method of claim 1wherein the strained channel layer comprises Si.

5. ~~11.~~ The method of claim 1 wherein x is approximately equal to y.

6. ~~12.~~ The method of claim ~~11~~ 5 wherein step (a) further comprises providing a sacrificial Si layer on said $Si_{1-y}Ge_y$ layer.

A4 7. ~~13.~~ The method of claim 1 wherein $y > x$.

8. ~~14.~~ The method of claim ~~13~~ 7 wherein step (a) further comprises providing a sacrificial Si layer on said $Si_{1-y}Ge_y$ layer.

9. ~~15.~~ The method of claim ~~14~~ 8 wherein step (a) further comprises providing a sacrificial Si layer on said $Si_{1-y}Ge_y$ layer having a thickness greater than the critical thickness.

10. ~~16.~~ The method of claim 1 wherein said substrate comprises Si.

11. ~~17.~~ The method of claim 1 wherein said substrate comprises Si having a layer of SiO_2 thereon.

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A4 Cancel'd 12. ~~18.~~ The method of claim 1 wherein said substrate comprises a SiGe graded buffer layer on Si.

13. ~~20.~~ A method of fabricating a semiconductor device comprising:

(a) providing a semiconductor heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer on said strained channel layer;

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(b) removing said $Si_{1-y}Ge_y$ layer to expose said strained channel layer;

and

(c) providing a dielectric layer on said exposed strained channel layer.

21. (Cancelled)

14. ~~22.~~ The method of claim ~~20~~ 13 wherein step (c) comprises forming the gate dielectric of a MISFET by providing a dielectric layer on said exposed strained channel layer.

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15. ~~23.~~ The method of claim ~~22~~ 14 wherein step (c) comprises forming the gate dielectric of a MISFET by providing an oxide on said exposed strained channel layer.

A7 16. ~~26.~~ The method of claim ~~20~~ 13 wherein said strained channel comprises Si.

17. ~~32.~~ The method of claim ~~20~~ 13 wherein said substrate comprises Si.

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18. ~~33.~~ The method of claim ~~20~~ 13 wherein said substrate comprises Si having a layer of SiO_2 thereon.

19 ~~34.~~ The method of claim ~~20~~ 13 wherein said substrate comprises a SiGe graded buffer layer on Si.

20. ~~36.~~ A method of fabricating a semiconductor device comprising the steps of:

(a) providing a semiconductor heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

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(b) removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

(c) providing a dielectric layer on said Si layer.

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21. ~~40.~~ The method of claim ~~3~~ 2 wherein oxidizing of at least a portion of said $Si_{1-y}Ge_y$ layer is performed using a wet oxidation technique.

22. ~~41.~~ The method of claim ~~40~~ 21 wherein said wet oxidation technique is utilized at a temperature up to about 750°C.

A10 23. ~~42.~~ The method of claim ~~20~~ 13 wherein step (b) comprises removing said $Si_{1-y}Ge_y$ layer to expose said strained channel layer using either wet or dry etch technique.

24. ~~43.~~ The method of claim ~~20~~ 13 further comprising the step of removing at least a portion of the strained channel layer to eliminate residual Ge.

25. ~~44.~~ The method of claim ~~36~~ 20 wherein step (b) comprises removing said $Si_{1-w}Ge_w$ layer to expose said Si layer using either wet or dry etch technique.

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